

**STATUS OF THE CLAIMS**

1. (previously presented) A memory cell, comprising two gated vertically stacked bipolar transistors configured to exhibit two bistable current states for storing information, one of said current states being achieved by operation of gate-induced latchup of said transistors, said two transistors respectively including a first gate and a second gate operational to induce said latchup, said first and second gates being connected to a respective first vertical side and a second vertical side of said vertically stacked bipolar transistors.

2. (previously presented) The memory cell of claim 1 wherein said gated vertically stacked bipolar transistors comprise two complementary vertical bipolar transistors.

3. (previously presented) The memory cell of claim 2 wherein said complementary bipolar transistors comprise a p-n-p transistor and an n-p-n transistor, said p-n-p transistor and said n-p-n transistor sharing their central n- and p-regions.

4. (previously presented) The memory cell of claim 3 wherein said first gate spans the central n-region of said p-n-p transistor.

5. (previously presented) The memory cell of claim 4 wherein said second gate spans the p-region of said n-p-n transistor.

6. (cancelled).

7. (previously presented) The memory cell of claim 6 wherein said first and second gates are orthogonally positioned relative to each other.

8. (original) The memory cell of claim 1 wherein said cell is a static random access memory cell.

9. (original) The memory cell of claim 1 wherein said cell has an area of about  $4F^2$  where F is the minimum lithographic dimension.

10. (previously presented) A circuit for storing information as one of at least two possible bistable current states, comprising at least one vertical p-n-p-n structure containing a bipolar p-n-p transistor merged with a bipolar n-p-n transistor at central n- and p-regions of said structure;

a first transistor gate spanning the central n-region of said p-n-p transistor on a first vertical side of said p-n-p-n structure; and

a second transistor gate spanning the central p-region of said n-p-n transistor on a second vertical side of said p-n-p-n structure that is orthogonal to said first vertical side.

11. (previously presented) The circuit of claim 10 wherein said transistor gates are configured to latch-up said p-n-p-n structure, wherein said latch-up results in one of said bistable current states.

12. (previously presented) The memory cell of claim 11 wherein said latch-up results in said memory cell having a lowered resistance.

13. (original) The circuit of claim 11 further comprising a substrate for supporting said vertical p-n-p-n structure.

14. (original) The circuit of claim 12 wherein said vertical p-n-p-n structure is disposed in a trench within said substrate.

15. (original) The circuit of claim 11 wherein said circuit is a static random access memory cell.

16. (original) The circuit of claim 14 wherein said memory cell has an area of about  $4F^2$  where F is the minimum lithographic dimension.

17. (previously presented) An SRAM cell, comprising:

a vertical transistor stack having a first p-region, a first n-region, a second p-region, and a second n-region;

a first gate bridging said first and second p-regions across the first n-region;

a second gate bridging said first and second n-regions across said second p-region;

a row address line in electrical communication with said first p-region;

a column address line in electrical communication with said second n-region;

a write row address line forming a first gate for gating charge between said first and second p-regions; and

a column write address line forming a second gate for gating charge between said first and second n-regions, wherein said first and second gates are configured to produce latch-up in said vertical transistor stack as a current state for storing information in said SRAM cell.

18. (previously presented) The SRAM cell of claim 17 wherein, said first and second gates are configured to produce latch-up when a voltage pulse is provided in both said first and second gates.

19. (previously presented) The memory cell of claim 18 wherein said first and second gates are positioned orthogonally to each other.

20. (original) The SRAM cell of claim 17 further comprising a substrate for supporting said p-n-p-n transistor and wherein said p-n-p-n transistor is a vertical structure disposed within a trench in said substrate.

Claims 21-22 (cancelled).

23. (previously presented) An SRAM array, comprising

a substrate;

a plurality of vertical transistors, each of said transistors being merged p-n-p and n-p-n transistors;

a first set of isolation trenches between said vertical transistors configured to isolate said vertical transistors in a first direction;

a second set of isolation trenches orthogonal to said first set of trenches configured to isolate said vertical transistors in a second direction;

a first gate line in at least some trenches of said first set of isolation trenches, said first gate line connecting central n-regions of at least some of said vertical transistors;

a second gate line in at least some of said trenches of said second set of isolation trenches, said second gate line connecting central p-regions of at least some of said vertical transistors; and

a third gate line not located in an isolation trench, said third gate line connecting upper n-regions of at least some of said vertical transistors.

24. (previously presented) The SRAM array of claim 23 further comprising an insulating material layer between each of said vertical transistors and the substrate, said insulating material at least partially isolating the vertical transistors.

25. (original) The SRAM array of claim 24 wherein said insulating material is an oxide.

26. (original) The SRAM array of claim 24 wherein said insulating material is a buried n-type layer.

27. (previously presented) The SRAM array of claim 23 wherein said plurality of vertical transistors are inverted and are supported by a p-type substrate.

28. (previously presented) A computer system, comprising

a processor; and

a memory circuit connected to the processor, the memory circuit containing at least one memory cell comprising two gated complementary bipolar transistors and having bistable current states for storing information, one of said current states being achieved by operation of gate-induced latch-up of said transistors, wherein the complementary bipolar transistors comprise a vertical p-n-p transistor and a vertical n-p-n transistor and the collector region of said p-n-p transistor is connected with the base region of said n-p-n transistor.

29. (previously presented) The computer system of claim 28, wherein said p-n-p transistor has a first gate spanning the n-region of said p-n-p transistor, and said n-p-n transistor has a second gate spanning the p-region of said n-p-n transistor.

30. (previously presented) The computer system of claim 28, wherein said transistors respectively further comprise a first gate and a second gate configured to induce latchup of said transistors when both said gates are turned on.

31. (previously presented) The computer system of claim 30 wherein said first and second gates are positioned adjacent to said transistors and orthogonal to each other.

32. (original) The computer system of claim 28 wherein said memory cell is a static random access memory cell.

33. (original) The computer system of claim 32 wherein said static random access memory cell has an area of about  $4F^2$  where F is the minimum lithographic dimension.

Claims 34-54 (cancelled).

55. (previously presented) The SRAM array of claim 23, further comprising a fourth gate line not located in an isolation trench, said fourth gate line connecting lower p-regions of at least some of said vertical transistors.